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Influence of driving and parasitic parameters on the switching behaviors of the SiC MOSFET

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The SiC MOSFET has lower conduction loss and switching loss than the Si IGBT, which helps to improve the efficiency and power density of the converter, especially for those having strict requirements for volume and weight, for example, electrical vehicles (EVs), on-board chargers (OBCs), and traction drive systems (TDS). However, the faster switching speed will cause overshoot and oscillation problems, which will affect the efficiency and security of the SiC devices and power electronic systems. For the SiC MOSFET to be better used, combining a theoretical analysis, the double-pulse test platform is built. The controllable principles of SiC MOSFETs are validated. The turn-on and turn-off delay, switching delay, switching di/dt, switching du/dt, switching overshoot, and switching loss of SiC MOSFETs under different driving and parasitic parameters are explored. Finally, some valuable suggestions for designing are proposed for a better application of the SiC MOSFET.

KEYWORDS

SiC MOSFET, parasitic parameter, driving parameter, overshoot, oscillation

1 Introduction

The SiC MOSFET is a typical wide-bandgap power semiconductor device (Zeng and Li, 2018). Compared with the Si IGBT, the SiC MOSFET has lower conduction loss and switching loss, which means the efficiency of the converter can be improved, especially in high-frequency applications. At the same time, the operation temperature of the SiC MOSFET is higher than that of the Si IGBT, which reduces the size of the heat sink, so the power density of the converter can be improved too. Therefore, the SiC MOSFET is considered to have potential in electric vehicles, photovoltaic power generation, and high-frequency power supplies (Camacho et al., 2017; Xie et al., 2021). However, due to the high switching speed of the SiC MOSFET, the current and voltage overshoot would reduce the electromagnetic compatibility of the converter. In addition, the overshoots and oscillations will accelerate the aging of the device and eventually cause its failure (Sun et al., 2021).

Various literature works studied the overshoots and oscillations of the SiC MOSFET during the switching transients. The influence of the source inductance and drain inductance on the overshoots is reported in Li et al. (2016) and Yang et al. (2022).

TABLE 1 Comparison of key parameters between the SiC MOSFET and Si IGBT.

	SiC MOSFET	Si IGBT
Name	C2M0080120D	IXGH20N120B
Breakdown voltage	1,200 V	1,200 V
Continuous current	36 A	40 A
On-state characteristics	80 mΩ	2.9 V
Gate charge	62 nC	72 nC
Input capacitance	950 pF	1,700 pF
Turn-on loss	265 μJ	2,100 μJ
Turn-off loss	135 μJ	3,500 μJ

TABLE 2 Influences of circuit parameters on the switching behaviors.

	$(di/dt)_{on}$	$(dv/dt)_{on}$	$(di/dt)_{off}$	$(dv/dt)_{off}$	E_{on}	E_{off}
$R_g\uparrow$		↓	↓	↓		↑
$C_{gs}\uparrow$	↓	-	↓	-	↑	↑
$C_{gd}\uparrow$	-	↓	-	↓	↑	↑
$C_{ds}\uparrow$	-	↓	-	↓	↑	↑
$L_{loop}\uparrow$	↑	-	↑	-		↑
$L_s\uparrow$	↓	-	↓	-	↑	↑

Considering different parasitic parameters, Bonyadi et al. (2015), Wang et al. (2019), and Talesara et al. (2020) provided the behavior model of the half bridge applying SiC MOSFETs, and the simulation and experiment results show that the overshoots and oscillations are mainly caused by the parasitic inductance in the loop, which should be reduced as much as possible. The analytical model is proposed in Stark et al. (2021) to characterize the switching behaviors of the SiC MOSFET. Riccio et al. (2018) confirmed that the gate driving resistor can damp the oscillation of the SiC MOSFET. However, comprehensive research about the influence of driving parameters and parasitic parameters on the switching behaviors of the SiC MOSFET is lacking among the existing studies, and there is no conductive guidance about designing the gate driver.

In this study, comprehensive research about the influence of driving parameters and parasitic parameters on the switching behaviors of the SiC MOSFET is carried out, which includes the gate resistance R_g, the gate–source capacitance C_{gs}, the gate–drain capacitance C_{gd}, the drain–source C_{ds}, the gate inductance L_g, the source inductance L_s, and the loop inductance L_{loop}. The measured results show that the switching behavior of the SiC MOSFET is controlled by these parameters from different aspects and should be given special attention during the designing period.

This paper is organized as follows. In Section 2, the switching behavior of the SiC MOSFET is studied. The dynamic characteristics of the SiC MOSFET with different driving and parasitic parameters are explained in Section 3. Finally, the conclusion is drawn in Section 4.

2 Switching behavior

2.1 Comparison between SiC and Si devices

The SiC MOSFET is considered a good substitute for the Si IGBT because better static and dynamic characteristics can be

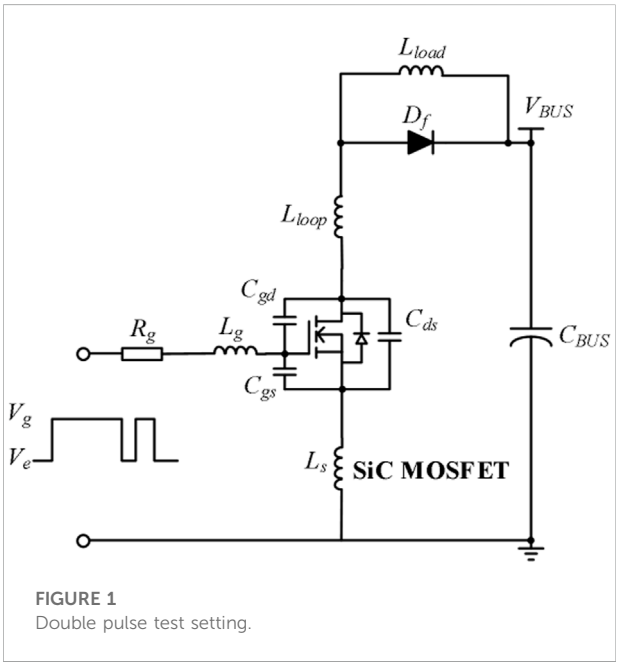

FIGURE 1
Double pulse test setting.

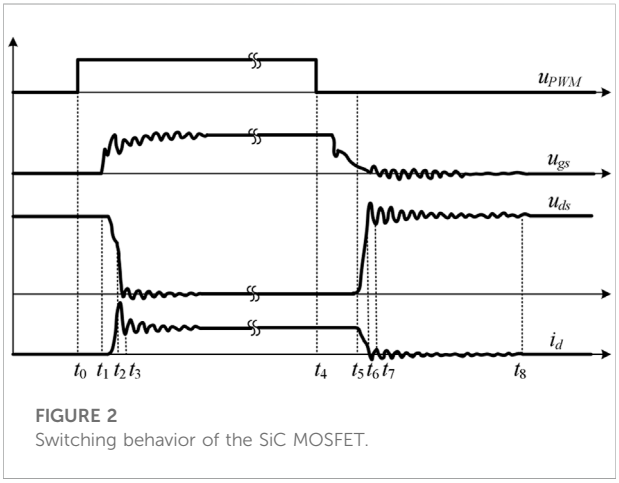

FIGURE 2
Switching behavior of the SiC MOSFET.

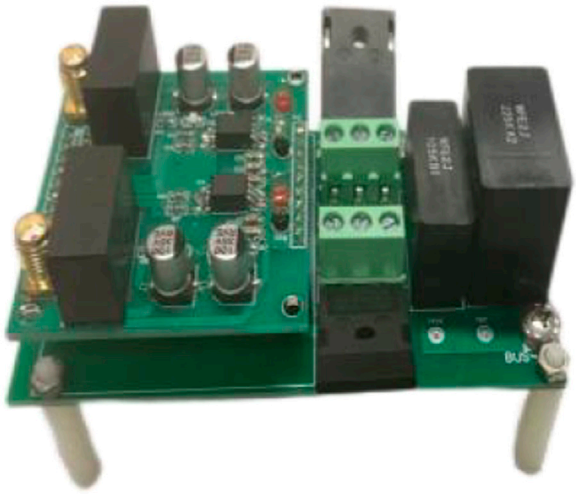

FIGURE 3
DPT prototype.

achieved in the SiC MOSFET. Table 1 shows the comparison of the key parameters between the SiC MOSFET and the Si IGBT. The Si IGBT (IXGH20N120B) and SiC MOSFET (C2M0080120D) are selected in the comparison because the power levels of the two devices are similar. In terms of the static characteristic, the on-state resistance of the SiC MOSFET is 80 mΩ, while the on-state voltage drop of the Si IGBT is 2.9 V, so the conduction loss of the SiC MOSFET is lower than that of the Si IGBT when the continuous conducting current is lower than 36.25 A. In terms of the dynamic characteristic, the gate charge and input capacitance of the SiC MOSFET are 62 nC and 950 pF, respectively, while those parameters of the Si IGBT are 72 nC and 1,700 pF, respectively. The lower gate charge and input capacitance of the SiC MOSFET mean that the SiC MOSFET can switch at a higher speed and frequency than those of the Si IGBT. It can be seen in Table 1 that the turn-on and turn-off switching losses of the SiC MOSFET are lower than those of the Si IGBT due to the high switching speed of the SiC MOSFET.

The high switching speed of the SiC MOSFET will cause overshoots, oscillations, and EMI during the ns-level switching transient. The driving parameters will influence the charging speed of the input capacitance, and the parasitic parameters will form resonant networks. In order to investigate the dynamic characteristics of the SiC MOSFET in detail, the double pulse test is carried out as follows.

2.2 Double pulse test

The dynamic characteristics of the power device are usually tested on the double pulse test (DPT) platform, which is built into PSpice software. The DPT setting is shown in Figure 1, where V_{BUS} is the bus voltage, C_{BUS} is the bus capacitor, L_{load} is the load inductor, D_f is the body diode of the SiC MOSFET, L_{loop} is the parasitic inductance in the loop, L_g is the inductance in the gate loop, L_s is the source inductance of the device, C_{gs} is the gate–source capacitance,

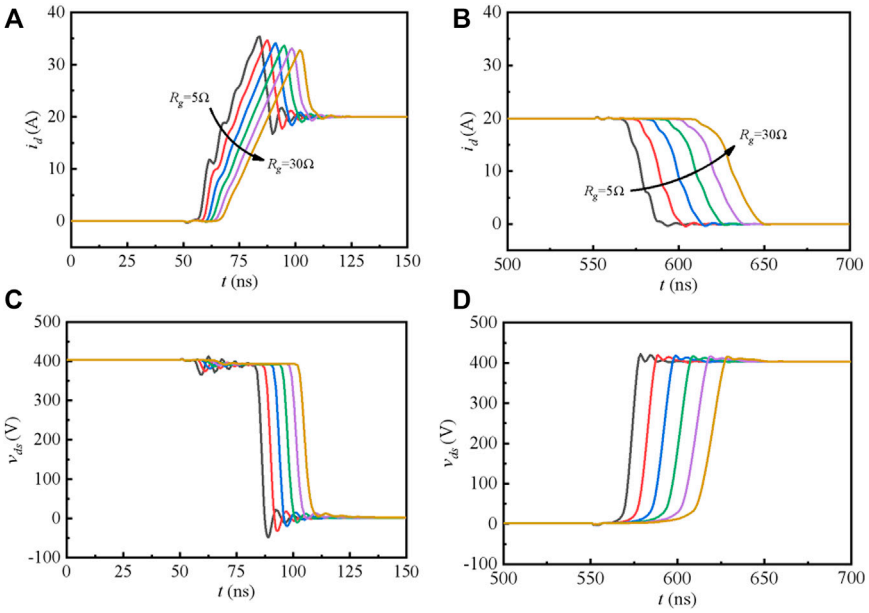

FIGURE 4
Influence of R_g on the switching behavior of the SiC MOSFET. **(A)** Turn-on i_d. **(B)** Turn-off i_d. **(C)** Turn-on u_{ds}. **(D)** Turn-off u_{ds}.

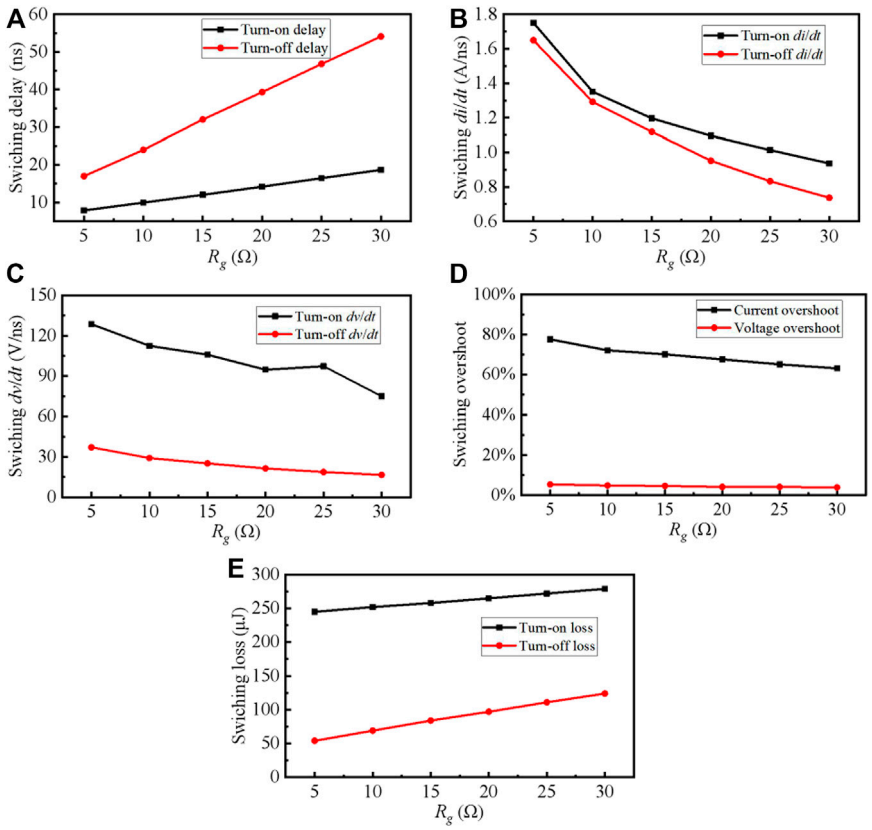

FIGURE 5
Dynamic characteristics of the SiC MOSFET with different R_g. **(A)** Switching delay. **(B)** Switching *di*/*dt*. **(C)** Switching *du*/*dt*. **(D)** Switching overshoot. **(E)** Switching loss.

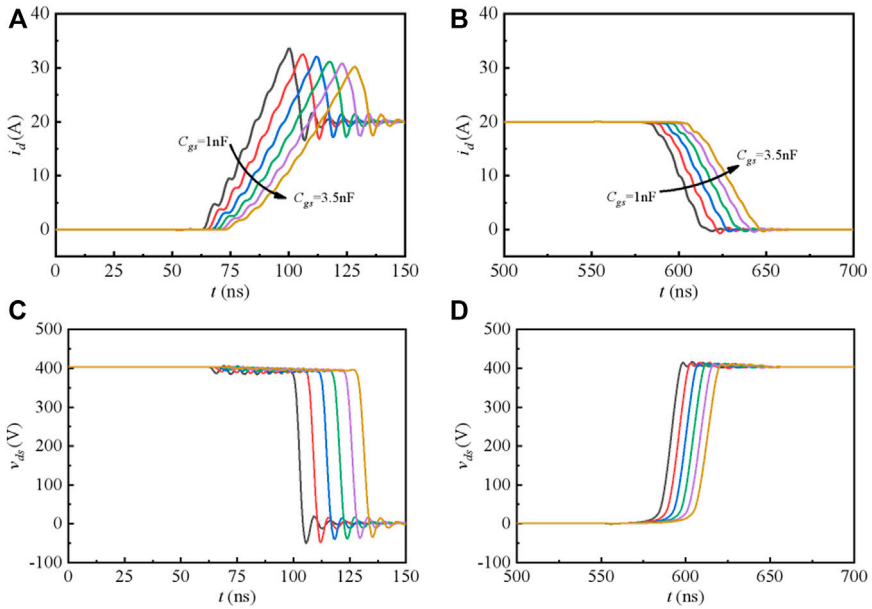

FIGURE 6
Influence of C_{gs} on the switching behavior of the SiC MOSFET. **(A)** Turn-on i_d. **(B)** Turn-off i_d. **(C)** Turn-on u_{ds}. **(D)** Turn-off u_{ds}.

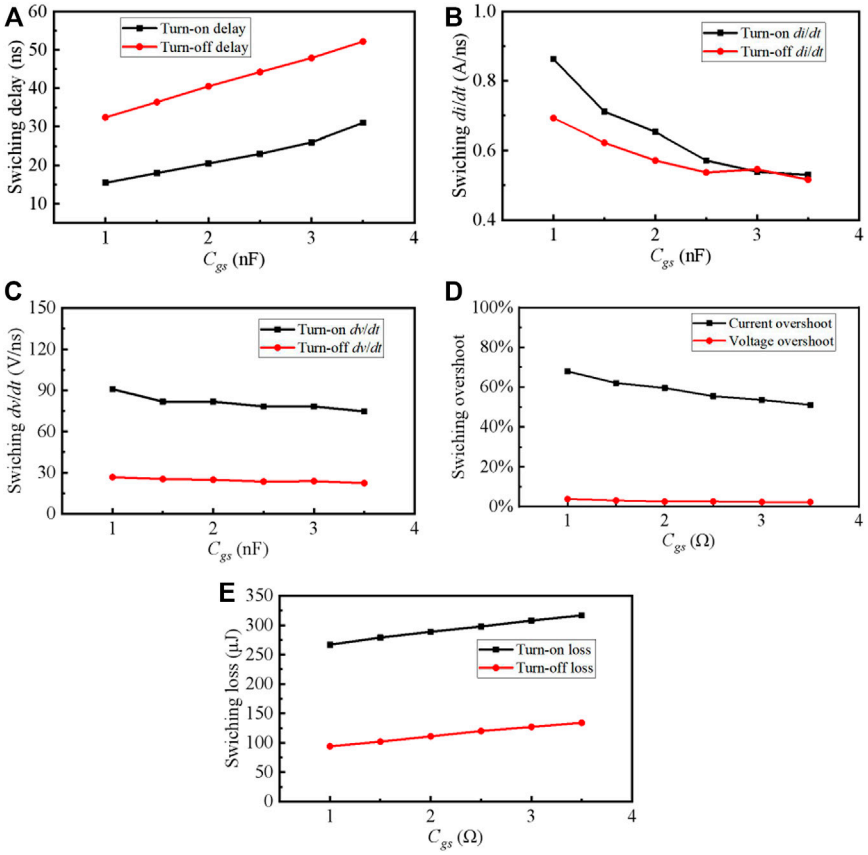

FIGURE 7
Dynamic characteristics of the SiC MOSFET with different C_{gs}. **(A)** Switching delay. **(B)** Switching di/dt. **(C)** Switching du/dt. **(D)** Switching overshoot. **(E)** Switching loss.

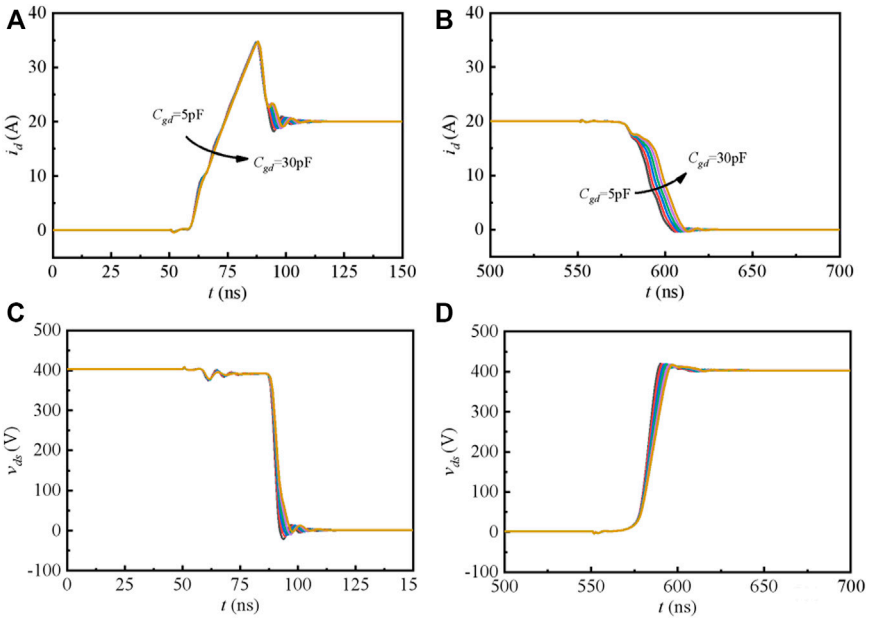

FIGURE 8
Influence of C_{gd} on the switching behavior of the SiC MOSFET. **(A)** Turn-on i_d. **(B)** Turn-off i_d. **(C)** Turn-on u_{ds}. **(D)** Turn-off u_{ds}.

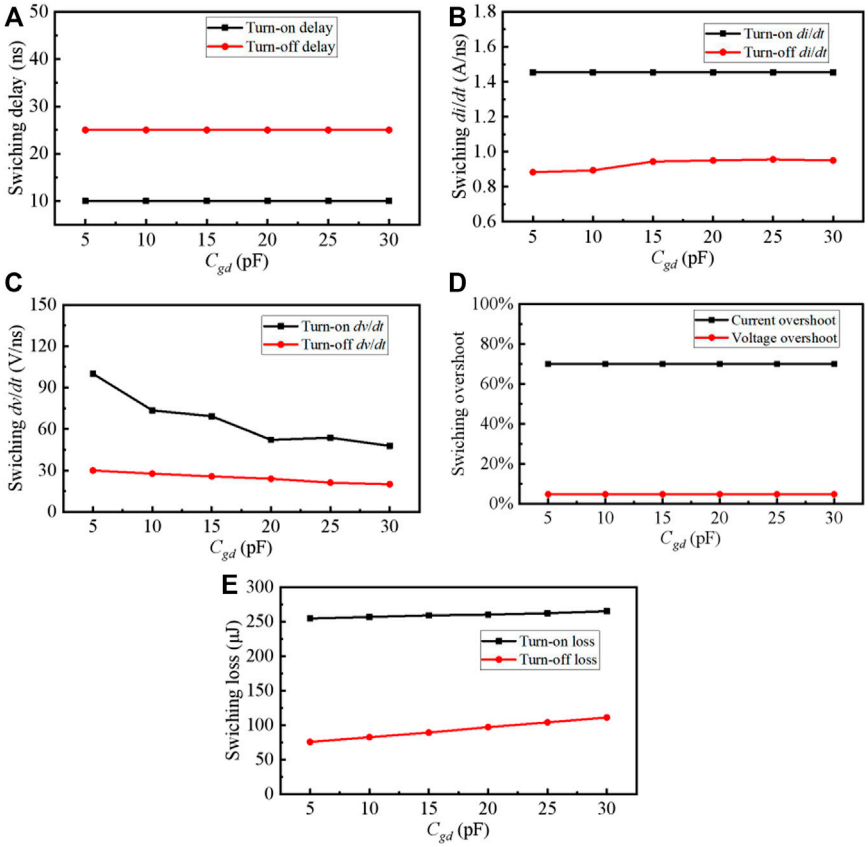

FIGURE 9
Dynamic characteristics of the SiC MOSFET with different C_{gd}. **(A)** Switching delay. **(B)** Switching *di*/*dt*. **(C)** Switching *du*/*dt*. **(D)** Switching overshoot. **(E)** Switching loss.

C_{gd} is the gate–drain capacitance, C_{ds} is the drain–source capacitance, R_g is the driving resistance, V_g is the positive driving voltage, and V_e is the negative driving voltage (Duan et al., 2018; Qin et al., 2018). The first driving pulse is used to establish the load current by turning on the SiC MOSFET, and the second pulse is used to observe the dynamic characteristics of the SiC MOSFET. It should be noted that R_g, C_{gs}, C_{gd}, and C_{ds} are changeable, and the parasitic inductances L_{loop}, L_g, and L_s are controllable during the design period.

2.3 Switching behaviors

The switching behavior of the SiC MOSFET can be represented by the waveforms of the gate–source voltage u_{gs}, the drain–source voltage u_{ds}, and the drain current i_d (Li et al., 2017; Huang et al., 2021; Xiong et al., 2022a). The key waveforms of the SiC MOSFET are shown in Figure 2.

It can be seen from Figure 2 that the turn-on behavior and turn-off behavior of the SiC MOSFET have the similar and symmetrical relationship. Both the turn-on and turn-off periods have five typical transients, namely, the delay period, the *di*/*dt* period, the *du*/*dt* period, the overshoot and oscillation period, and the state period (As detailed in Appendix A). The slew rate of the drain current is the cause of the overshoot for i_d and u_{ds}. In the turn-on transient, the reverse recovery of the body diode will cause the current overshoot, and it has

$$I_{peak} = \sqrt{\frac{2Q_{rr}\frac{di_d}{dt}}{S+1}}, \tag{1}$$

where I_{peak} is the peak value of i_d, Q_{rr} is the reverse recovery charge of the body diode, and S is the snappiness factor of the body diode. In the turn-off transient, the parasitic inductance in the loop will cause an obvious overshoot in u_{ds} (Wu et al., 2020; Zhao et al., 2020a; Qi et al., 2021), and it has

$$V_{peak} = L_{loop}\frac{di_d}{dt} + V_{BUS}. \tag{2}$$

The slew rate of the drain–source voltage u_{ds} is the cause for the crosstalk phenomena. When the SiC MOSFET switches at

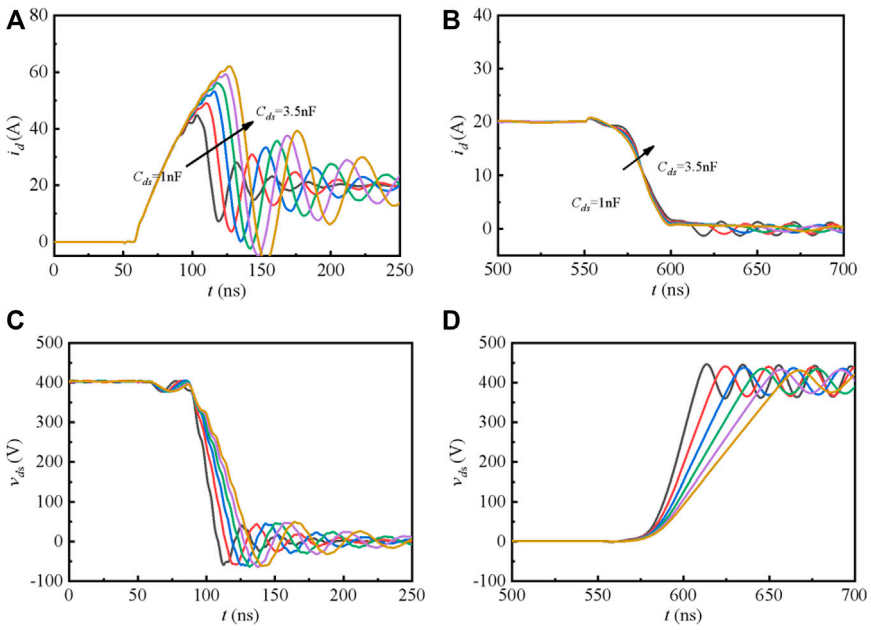

FIGURE 10
Influence of C_{ds} on the switching behavior of the SiC MOSFET. **(A)** Turn-on i_d. **(B)** Turn-off i_d. **(C)** Turn-on u_{ds}. **(D)** Turn-off u_{ds}.

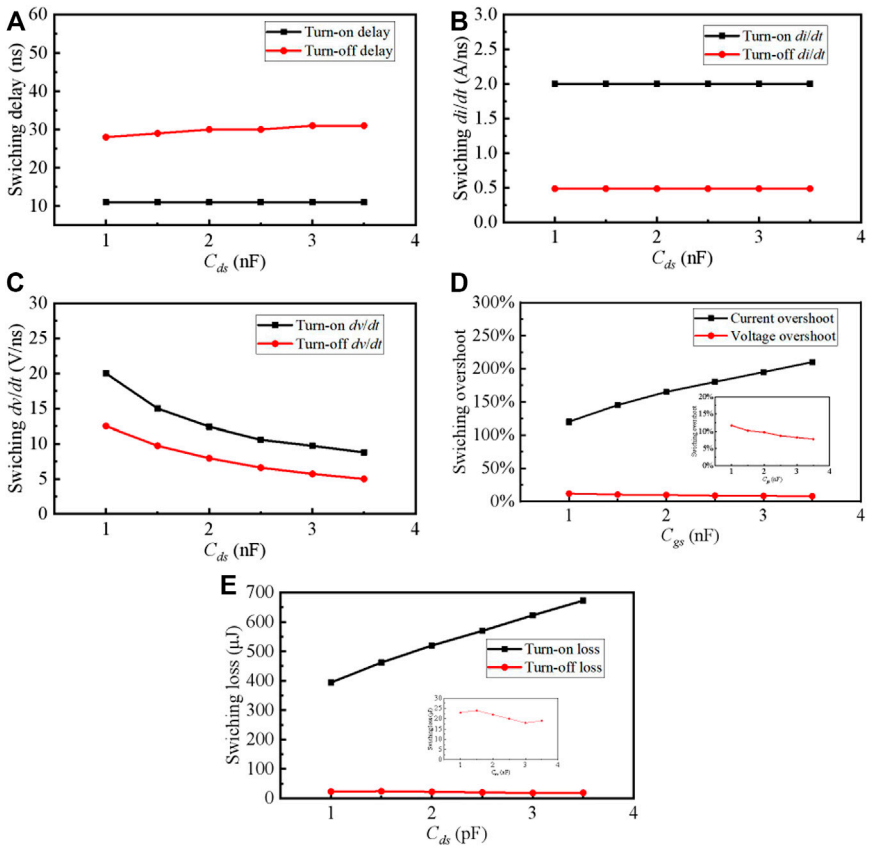

FIGURE 11
Dynamic characteristics of the SiC MOSFET with different C_{ds}. **(A)** Switching delay. **(B)** Switching *di*/*dt*. **(C)** Switching *du*/*dt*. **(D)** Switching overshoot. **(E)** Switching loss.

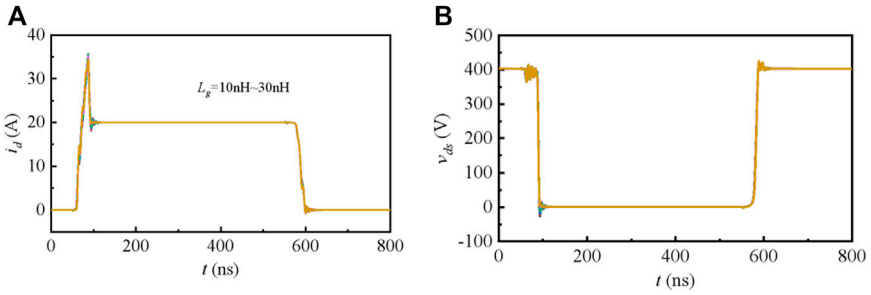

FIGURE 12
Influence of L_g on the switching behavior of the SiC MOSFET. **(A)** Turn-on and Turn-off of i_d. **(B)** Turn-off u_{ds}.

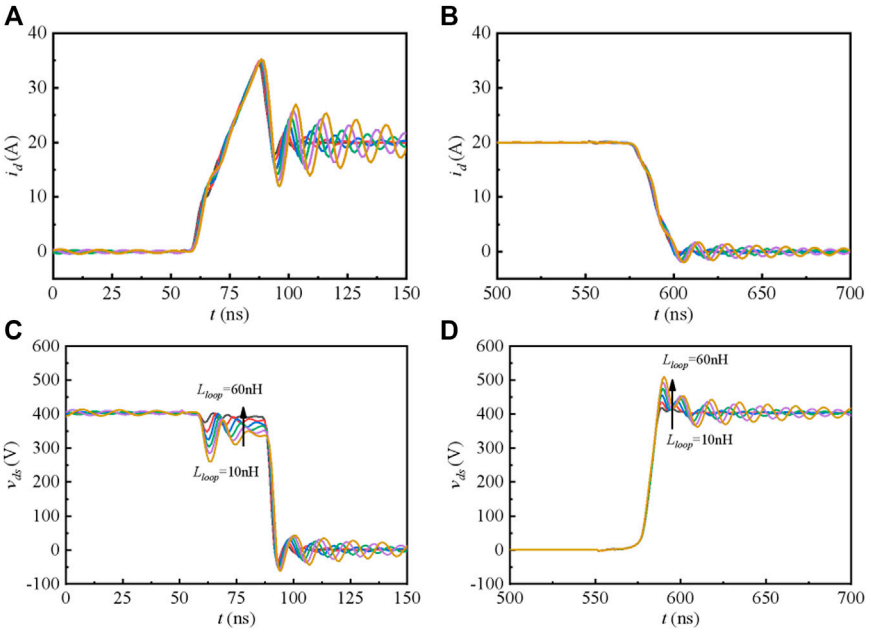

FIGURE 13
Influence of L_{loop} on the switching behavior of the SiC MOSFET. **(A)** Turn-on i_d. **(B)** Turn-off i_d. **(C)** Turn-on u_{ds}. **(D)** Turn-off u_{ds}.

high switch, the displacement current through C_{gd} will cause the false turn-on of the synchronization device (Roy and Basu, 2021), and the displacement current i_{gd} can be expressed as follows:

$$i_{gd} = C_{gd}\frac{du_{ds}}{dt}. \tag{3}$$

The switching behavior of the SiC MOSFET is directly related to the reliability of the device (Chen et al., 2021; Rashid et al., 2021). Therefore, it is important to carry out the comprehensive research about the influence of driving parameters and parasitic parameters on the switching behaviors of the SiC MOSFET.

3 Experiment results

The DPT prototype is applied to investigate the dynamic characteristics of the SiC MOSFET, as shown in Figure 3. The load inductance L_{load} is equal to 200 μH, the tested device is C2M0080120D of CREE, the bus voltage is equal to 400 V, and the load current is 20 A. The oscilloscope is DPO3054 (500 MHz), the current probe is TCP305 A (30 MHz), and the voltage probe is P6139 A (500 MHz). The bandwidth of the probe is enough for measuring the transients of u_{ds} and i_d.

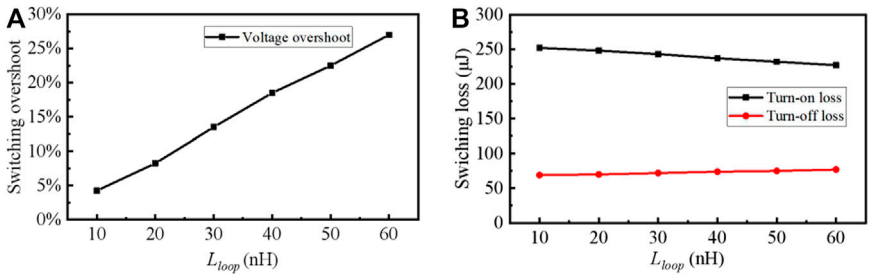

FIGURE 14
Dynamic characteristics of the SiC MOSFET with different L_{loop}. **(A)** Switching overshoot. **(B)** Switching loss.

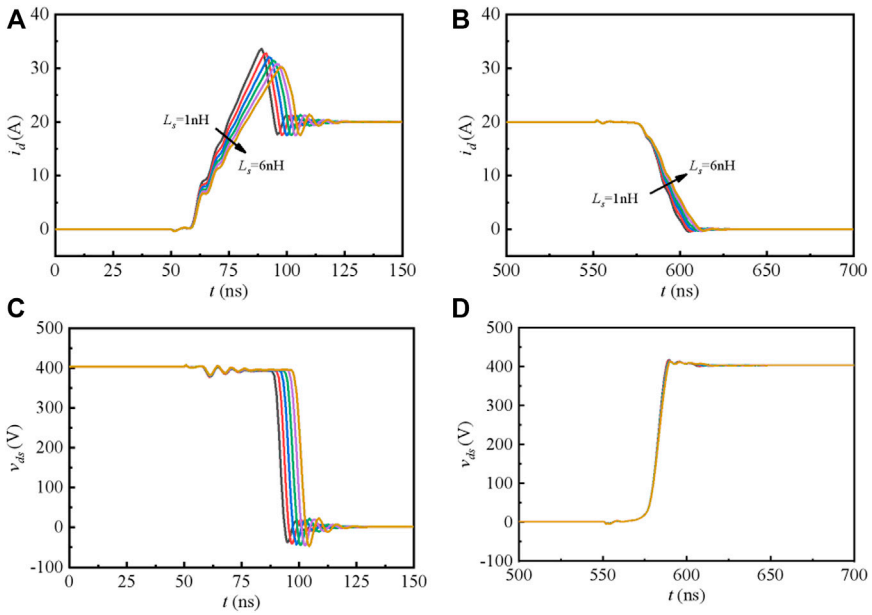

FIGURE 15
Influence of L_s on the switching behavior of the SiC MOSFET. **(A)** Turn-on i_d. **(B)** Turn-off i_d. **(C)** Turn-on u_{ds}. **(D)** Turn-off u_{ds}.

3.1 Influence of R_g

The gate driving R_g can be selected during the designing period. Figure 4 shows the waveforms of i_d and u_{ds} with different R_g, and Figure 5 presents the dynamic characteristics of the SiC MOSFET with different R_g. It is obvious that with the increase in R_g, the turn-on and turn-off delay of the device will increase because the charging time of the input capacitance increases. The slew rate of i_d and u_{ds} decreases with the increase of R_g, so the overshoot decreases and the device can operate at a slower speed. It is evident that both turn-on and turn-off losses increase with a larger R_g. Therefore, the worst efficiency of the converter occurs when a relatively large R_g is selected.

3.2 Influence of C_{gs}

The gate–source capacitance C_{gs} determines the delay time and the value of di/dt. As shown in Figure 6 and Figure 7, the influence of C_{gs} on the dynamic characteristics of the SiC MOSFET is similar to that of R_g. The switching speed will decrease if a larger C_{gs} is selected. It should be noted that the value of C_{gs} has no significant influence on the slew rate of u_{ds}.

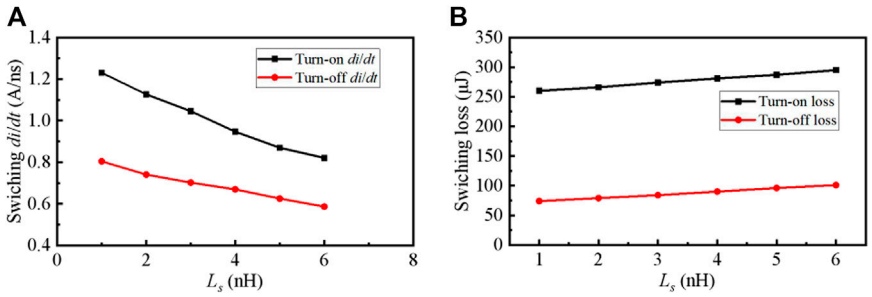

FIGURE 16
Dynamic characteristics of the SiC MOSFET with different L_s. **(A)** Switching *di*/*dt*. **(B)** Switching loss.

3.3 Influence of C_{gd}

The gate–drain capacitance C_{gd} determines the value of *du*/*dt*, which is also called the "Miller capacitance." The value of C_{gd} is far lower than the value of C_{gs} and C_{ds}, and a little change in C_{gd} will cause a significant change in the value of *du*/*dt*. Figure 8 shows the waveforms of i_d and u_{ds} with different C_{gd}, and Figure 9 presents the dynamic characteristics of the SiC MOSFET with different C_{gd}. It can be seen that delay and *di*/*dt* have no obvious relationship with the value of C_{gd}. However, *du*/*dt* will decrease with the increase of C_{gd}, which will cause an increase in switching losses in turn. It should be noted that though the value of *du*/*dt* decreases with a larger C_{gd}, no significant optimization of overshoot occurs, and the risk of false turn-on will increase.

3.4 Influence of C_{ds}

The drain–source capacitance C_{ds} can influence the value of *du*/*dt*, and there is no necessary relationship between C_{ds}, delay, and *di*/*dt*. The additional C_{ds} is applied to achieve the soft turn-off by increasing C_{ds}. As shown in Figure 10 and Figure 11, both turn-on and turn-off *du*/*dt* will decrease with the increase of C_{ds}, and the turn-off loss and turn-off voltage overshoot will decrease as a result. However, the energy stored in C_{ds} during the turn-off period will cause a significant current overshoot during the turn-on period, which means an obvious increase in the turn-on loss.

3.5 Influence of L_g

The gate inductance L_g is caused by the PCB trace of the gate loop. As shown in Figure 12, the value of L_g has a minor influence on the dynamic characteristics of the SiC MOSFET. However, L_g should be reduced as much as possible because L_g will result in the overshoot of u_{gs}, which risks the reliability of the gate.

3.6 Influence of L_{loop}

The gate inductance L_{loop} is caused by the PCB trace of the power loop. It is different to cancel the L_{loop}, even though the relatively short PCB trace is designed. The most significant drawback brought by L_{loop} is the larger voltage overshoot, which will cause the device to breakdown. As shown in Figure 13 and Figure 14, the value of L_{loop} only influences the oscillation frequency and the voltage overshoot. In order to enhance the reliability of the SiC MOSFET, L_{loop} should be reduced as much as possible. It should be noted that a larger L_{loop} will result in lower turn-on loss because the drain–source voltage will drop during the *di*/*dt* period. At the same time, the turn-off loss will increase with the larger L_{loop} due to the additional loss from the voltage overshoot.

3.7 Influence of L_s

The source inductance L_s exists in the gate loop and the power loop. As shown in Figure 15 and Figure 16, when the drain current i_d changes sharply, the induced voltage on L_s will slow down the switching speed as a negative feedback effect. Therefore, the larger L_s will cause lower *di*/*dt* during the switching transients. In order to reduce the switching losses, new type packages are provided by manufacturers, such as TO-247-4 and TO-263-7.

4 Conclusion

The SiC MOSFET is widely used in high-frequency and high-temperature applications, which helps to improve the efficiency and power density of the converter. However, the parasitic parameters will inevitably cause overshoot and oscillation of i_d and u_{ds}, which reduce the reliability of the SiC MOSFET. In this study, comprehensive research about the influence of driving parameters and parasitic parameters on the switching behaviors of the SiC MOSFET is carried out, and some valuable conclusions drawn are as follows:

1) The parasitic inductance should be reduced as much as possible by optimizing PCB traces and applying advanced packages
2) Different driving parameters will cause different dynamic responses of the SiC MOSFET, which should be considered according to special applications, respectively
3) The increase in C_{gd} is not recommended due to the higher risk of crosstalk

The influences of circuit parameters on the switching behaviors of the SiC MOSFET are listed as shown in Table 2.

Data availability statement

The original contributions presented in the study are included in the article/Supplementary Material; further inquiries can be directed to the corresponding author.

Author contributions

SZ: conceptualization, formal analysis, data curation, writing—original draft, visualization, and funding acquisition.

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Conflict of interest

The author declares that the research was conducted in the absence of any commercial or financial relationships that could be construed as a potential conflict of interest.

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Appendix A:

The turn-on current oscillation and the turn-off voltage oscillation are two critical phenomena when describing the switching behaviors of the SiC MOSFET (Li et al., 2020). The turn-on current resonance angle frequency and the resonance damping of the SiC MOSFET can be expressed as follows:

$$\omega_{on} = \frac{1}{\sqrt{L_{loop}\left(C_{oss} + C_L\right)}}, \tag{4}$$

$$\xi_{on} = \frac{R_{ds\_on}\left(C_{oss} + C_L\right)}{2\omega_{on}}. \tag{5}$$

The turn-off voltage resonance angle frequency and the resonance damping of the SiC MOSFET can be expressed as follows (Liu et al., 2016; Mukunoki et al., 2018):

$$\omega_{off} = \frac{1}{\sqrt{L_{loop}\left(C_{oss} + C_L\right)}}, \tag{6}$$

$$\xi_{off} = \frac{R_F}{2}\frac{1}{\omega_{off}L_{loop}} = \frac{R_F}{2}\sqrt{\frac{C_F + C_L}{L_{loop}}}, \tag{7}$$

where C_L is the output capacitance of the freewheeling diode and R_L is the equivalent on-state resistance of the freewheeling diode.